? show files

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File 347:JAPIO Dec 1976-2009/Nov(Updated 100228)
         (c) 2010 JPO & JAPIO
File 350:Derwent WPIX 1963-2010/UD=201019
         (c) 2010 Thomson Reuters
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? ds

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Set     Items   Description
S1     809340   (ADDRESS? ? OR LINK OR (WEB OR FTP OR WWW OR HTTP)(1W)SERV-
              ER? ? OR NAME? ?(1N)SERVER? ? OR DNS OR (IP OR INTERNET()PROT-
              OCOL)()ADDRESS?? OR (HOST OR DOMAIN)()NAME? ? OR SERVER()(ID -
              OR IDENTIFICATION))
S2       4069   S1(3N)(BACKUP OR BACK()UP OR SECONDARY OR REDUNDANT)
S3     126209   (POSITION? ?  OR LOCATION? ?  OR OFFSET OR OFF()SET)(3N)(F-
              IELD? ? OR ARRAY? ? OR STORAGE? ? OR MEMORY OR MEMORIES OR ME-
              DIA OR MEDIUM OR MEDUIM)
S4      66109   S1(3N)(MULTI OR MANY OR TWO OR MULTIPL? OR SEVERAL OR MANY
              OR PLURAL? OR RANGE? ? OR ASSORT? OR SERIES OR VARIOUS OR MOR-
              E(3W)(ONE OR 1))
S5        900   S3(10N)S4
S6          8   S5(20N)S2
S7         18   S5 AND S2
S8         14   S7 AND PY=1963:2003
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Subject summary

? t/ 3,k/ all

Dialog eLink: Order File History
8/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0013266467 *Drawing available*
WPI Acc no: 2003-352252/**200333**
XRPX Acc No: N2003-281309
Multiplexing apparatus for cache memory system, selects bitline having predetermined data values in response to possible subsequences of bit values identified by pre-decoder
Patent Assignee: INTEL CORP (ITLC)
Inventor: ZHANG K X

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 6507531	B1	20030114	US 2000538553	A	20000329	200333	B

Priority Applications (no., kind, date): US 2000538553 A 20000329

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 6507531	B1	EN	26	16	

Alerting Abstract ...NOVELTY - A pre-decoder receives an **address** in **redundant** form and identifies subsequences of bit values corresponding to digit positions in the **redundant address**. A column multiplexer receives data values on respective portion of bitline and selects bitline in... Original Publication Data by AuthorityArgentina**Publication No.** ...**Claims:**An apparatus comprising:a plurality of storage locations associated with a plurality of bitlines;a **pre**-decoder to receive an **address** in **redundant** form and to identify one or more possible **subsequences** of **bit** values corresponding to each of a plurality of digit positions in the **redundant address**; anda first column multiplexer having a first bitline **output**, **the** first column multiplexer to receive a first plurality of data values on a first portion... ... Basic Derwent Week: **200333**...

Dialog eLink: Order File History
8/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0013218452
WPI Acc no: 2003-303165/**200330**
XRPX Acc No: N2003-241072
Extending method for instruction set of central processing unit (CPU) of electronic device identifying and retrieving portion of data from memory, manipulating portion of data and saving manipulated data in the memory
Patent Assignee: PACE MICRO TECHNOLOGY PLC (PACE-N)
Inventor: BALDOCK M; HEMMING S

Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
GB 2379531	A	20030312	GB 200211310	A	20020517	200330	B
GB 2379531	B	20050525				200536	E

Priority Applications (no., kind, date): GB 200114592 A 20010614

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
GB 2379531	A	EN	9	0	

Alerting Abstract ...NOVELTY - The method involves identifying each **location** in a **memory** by a unique **address** consisting of **several** bits in an **address** word. The method involves identifying and retrieving a portion of data from the memory, manipulating... ...ADVANTAGE - Extends instruction set of existing word architecture by using **redundant address** bits to provide instructions for atomic/uninterrupted operations to be performed during operations such as ... ... Basic Derwent Week: **200330**...

Dialog eLink: Order File History
8/3,K/3 (Item 3 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0013010942 *Drawing available*
WPI Acc no: 2003-089210/**200308**
Related WPI Acc No: 1998-413465; 1999-632781; 2001-089769
XRPX Acc No: N2003-070263
Semiconductor memory chip e.g. DRAM testing method involves testing primary and redundant memory elements, based on redundant memory element select signal and compressed address signals
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: MERRITT T A

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 6452845	B1	20020917	US 1999227483	A	19990107	200308	B
			US 2000659247	A	20000911		

Priority Applications (no., kind, date): US 1999227483 A 19990107; US 2000659247 A 20000911

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 6452845	B1	EN	12	5	Continuation of application	US 1999227483
					Continuation of patent	US 6118711

Alerting Abstract ...ADVANTAGE - Since the addresses are compressed during testing, single **address** to access **multiple locations** in **memory array** is enabled. Hence, allows data to be written and read from multiple locations using a... Original Publication Data by AuthorityArgentina**Publication No.** ...**Claims:**receiving a select signal at an address terminal of the semiconductor memory device;generating a **redundant memory** element select signal in response to the externally received select signal; andaccessing and testing... ... and redundant memory elements responsive to the redundant memory element select signal and the compressed **externally** received **address** signals.Basic Derwent Week: **200308**

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8/3,K/4 (Item 4 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0012753974 *Drawing available*
WPI Acc no: 2002-607146/**200265**
Related WPI Acc No: 2000-363572; 2001-059461; 2002-589698; 2003-028169; 2003-287401
XRPX Acc No: N2002-480762
Row-column counter integrated memory for computer system, receives row and column addresses in generated physical and logical sequence based on which memory cell of memory circuit is selected
Patent Assignee: FISTER W E (FIST-I); MICRON TECHNOLOGY INC (MICR-N)
Inventor: FISTER W E

Patent Family (2 patents, 1 countries)							
Patent Number	**Kind**	**Date**	**Application Number**	**Kind**	**Date**	**Update**	**Type**
US 20020067646	A1	20020606	US 199883830	A	19980522	200265	B
			US 1999338257	A	19990622		
			US 2000632493	A	20000803		
			US 2001870982	A	20010530		
			US 200139785	A	20011026		
US 6538938	B2	20030325	US 199883830	A	19980522	200325	E
			US 1999338257	A	19990622		
			US 2000632493	A	20000803		
			US 2001870982	A	20010530		
			US 200139785	A	20011026		

Priority Applications (no., kind, date): US 199883830 A 19980522; US 1999338257 A 19990622; US 2000632493 A 20000803; US 2001870982 A 20010530; US 200139785 A 20011026

Patent Details						
Patent Number	**Kind**	**Lan**	**Pgs**	**Draw**	**Filing Notes**	
US 20020067646	A1	EN	9	3	Division of application	US 199883830
					Continuation of application	US 1999338257
					Division of application	US 2000632493
					Division of application	US 2001870982
US 6538938	B2	EN			Division of application	US 199883830
					Continuation of application	US 1999338257
					Division of application	US 2000632493
					Division of application	US 2001870982
					Division of patent	US 6049505
					Continuation of patent	US 6104669
					Division of patent	US 6452868
					Division of patent	US 6483773

Original Publication Data by AuthorityArgentina**Publication No.** ...**Claims:**having a plurality of memory locations;a counter operable to generate a plurality of row **and column** addresses in a physical sequence; anda memory **address** selecting circuit coupled to the counter and operable to receive the row and column addresses... ... plurality of memory addresses as row addresses and column addresses from a plurality of row **address** sources and **column address** sources, respectively, the memory addresses being generated internal to the integrated and the memory addresses corresponding to primary and **redundant** memory cells, wherein **the** plurality of row address sources comprises a normal row address source defined by a row address applied to the integrated circuit, a refresh **row address** generation source, and a functional testing row address generation source;selecting one of the plurality of row address sources and column address sources; andaccessing the primary **and redundant** memory cells corresponding to the selected row and column address sources.... Basic Derwent Week: **200265**...

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8/3,K/5 (Item 5 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0012737094 *Drawing available*
WPI Acc no: 2002-589698/**200263**
Related WPI Acc No: 2000-363572; 2001-059461; 2002-607146; 2003-028169; 2003-287401
XRPX Acc No: N2002-467941
Integrated memory device e.g. DRAM used in computer system, receives row and column addresses

of redundant and non-redundant memory spaces, based on which memory location is selected
Patent Assignee: FISTER W E (FIST-I); MICRON TECHNOLOGY INC (MICR-N)
Inventor: FISTER W E

Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20020075749	A1	20020620	US 199883830	A	19980522	200263	B
			US 1999338257	A	19990622		
			US 2000632493	A	20000803		
			US 2001870982	A	20010530		
			US 200116721	A	20011029		
US 6510102	B2	20030121	US 199883830	A	19980522	200309	E
			US 1999338257	A	19990622		
			US 2000632493	A	20000803		
			US 2001870982	A	20010530		
			US 200116721	A	20011029		

Priority Applications (no., kind, date): US 199883830 A 19980522; US 1999338257 A 19990622; US 2000632493 A 20000803; US 2001870982 A 20010530; US 200116721 A 20011029

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 20020075749	A1	EN	10	3	Division of application	US 199883830
					Continuation of application	US 1999338257
					Division of application	US 2000632493
					Division of application	US 2001870982
US 6510102	B2	EN			Division of application	US 199883830
					Continuation of application	US 1999338257
					Division of application	US 2000632493
					Division of application	US 2001870982
					Division of patent	US 6049505
					Continuation of patent	US 6104669

Original Publication Data by AuthorityArgentina**Publication No.** ...**Claims:**having a plurality of memory locations; a counter operable to generate a plurality of row **and column** addresses in a physical sequence; and a memory **address** selecting circuit coupled to the counter and operable to receive the row and column addresses... ... the memory device and the memory addresses corresponding to memory cells in the primary and **redundant memory** spaces, wherein the plurality of row address sources comprises a normal row address source defined by a row address applied to the memory device, a refresh row **address generation** source, and a functional testing row address generation source; selecting one of the plurality of row address sources and column address sources; and accessing the memory cells in **the** primary and **redundant** memory spaces corresponding to the selected row and column address sources. Basic Derwent Week: **200263**

Dialog eLink: Order File History
8/3,K/6 (Item 6 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0010533808 *Drawing available*
WPI Acc no: 2001-136217/**200114**
XRPX Acc No: N2001-099034
Matched addresses analysis apparatus for content addressable memory, produces control signal for analyzing each detected match existing between input data and stored data
Patent Assignee: VLSI TECHNOLOGY INC (VLSI-N)
Inventor: MARTIN W C

Patent Family (1 patents, 1 countries)							
Patent Number	**Kind**	**Date**	**Application Number**	**Kind**	**Date**	**Update**	**Type**
US 6118682	A	20000912	US 1998110872	A	19980707	200114	B

Priority Applications (no., kind, date): US 1998110872 A 19980707

Patent Details					
Patent Number	**Kind**	**Lan**	**Pgs**	**Draw**	**Filing Notes**
US 6118682	A	EN	7	2	

Original Publication Data by AuthorityArgentina**Publication No. Claims:**An apparatus comprising:an addressable storage device having a **plurality** of addressable **locations for** storing data;an **address** encoder for selectively addressing **secondary memory locations** in response to outputs of said addressable storage device; anda control device for examining... ... Basic Derwent Week: **200114**...

Dialog eLink: Order File History
8/3,K/7 (Item 7 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0010034000 *Drawing available*
WPI Acc no: 2000-338793/**200029**
XRPX Acc No: N2000-254325
Address decoder for memory, receives address data signals in redundant form and memory line in memory is organized into two blocks which are coupled to address decoder by enable lines
Patent Assignee: INTEL CORP (ITLC)
Inventor: SAGER D J; SAGER J

Patent Family (11 patents, 25 countries)							
Patent Number	**Kind**	**Date**	**Application Number**	**Kind**	**Date**	**Update**	**Type**
WO 2000017757	A2	20000330	WO 1999US27873	A	19990827	200029	B
US 6172933	B1	20010109	US 1998148314	A	19980904	200104	E
EP 1129409	A2	20010905	EP 1999965886	A	19990827	200151	E
			WO 1999US27873	A	19990827		
TW 440830	A	20010616	TW 1999113238	A	19990803	200203	E
KR 2001073124	A	20010731	KR 2001702859	A	20010305	200209	E
CN 1325533	A	20011205	CN 1999812853	A	19990827	200223	E
KR 394136	B	20030809	WO 1999US27873	A	19990827	200413	E
			KR 2001702859	A	20010305		
EP 1129409	B1	20041124	EP 1999965886	A	19990827	200477	E
			WO 1999US27873	A	19990827		
DE 69922240	E	20041230	DE 69922240	A	19990827	200502	E
			EP 1999965886	A	19990827		
			WO 1999US27873	A	19990827		
DE 69922240	T2	20051110	DE 69922240	A	19990827	200574	E
			EP 1999965886	A	19990827		
			WO 1999US27873	A	19990827		
CN 1199183	C	20050427	CN 1999812853	A	19990827	200641	E

Priority Applications (no., kind, date): US 1998148314 A 19980904

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
WO 2000017757	A2	EN	30	13		
National Designated States,Original	BR CN KR SG					
Regional Designated States,Original	AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 1129409	A2	EN			PCT Application	WO 1999US27873
					Based on OPI patent	WO 2000017757
Regional Designated States,Original	AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
TW 440830	A	ZH				
KR 394136	B	KO			PCT Application	WO 1999US27873
					Previously issued patent	KR 2001073124
					Based on OPI patent	WO 2000017757
EP 1129409	B1	EN			PCT Application	WO 1999US27873
					Based on OPI patent	WO 2000017757
Regional Designated States,Original	DE GB					
DE 69922240	E	DE			Application	EP 1999965886
					PCT Application	WO 1999US27873
					Based on OPI patent	EP 1129409
					Based on OPI patent	WO 2000017757
DE 69922240	T2	DE			Application	EP 1999965886
					PCT Application	WO 1999US27873
					Based on OPI patent	EP 1129409
					Based on OPI patent	WO 2000017757

Address decoder for memory, receives address data signals in redundant form and memory line in memory is organized into two blocks which are coupled to... ...**Original Titles:REDUNDANT** FORM **ADDRESS** DECODER FOR MEMORY SYSTEM... ...**REDUNDANT** FORM **ADDRESS** DECODER FOR MEMORY SYSTEM... ...**Redundant** form **address** decoder for memory system... ...**REDUNDANT** FORM **ADDRESS** DECODER FOR MEMORY SYSTEM **Alerting Abstract** ...NOVELTY - The memory system (200) has an address decoder (210) which receives **address** data signals in **redundant** form. A memory (220) has memory lines (222) and each memory line is organized into... ...zero delay decoding of address data in single addition implementation. Provides address decoder that decodes **address** data in **redundant** form. **Address** decoder permits arithmetic operations to be made on address data at very high speed, and... Original Publication Data by AuthorityArgentina**Publication No. Original Abstracts:**The present invention provides a memory system (200) that retrieves data based upon **redundant** form **address** data. **The** memory **system** (200) includes a memory (220) having a plurality of memory lines (222) and an address decoder (210) that enables one of the memory lines (222) in response to a **redundant** form **address** signal. **A redundant form** decoder (230) **decodes redundant** form data into a differential pair of decoded address lines for each bit **position** of a **memory address**. One of **the two** differential pairs carries **correct address** data. The one address line to be used is determined on a memory line by memory line basis, using the address of the memory **lines** themselves. The **redundant** form **address** decoder (**230**) avoids **a** completion add that would otherwise be required, yielding very fast access to memory... ... The present invention provides a memory system that retrieves data based upon **redundant** form **address** data. The **memory** system **includes** a memory having a plurality of memory lines and an address decoder that enables one of the memory lines in response to a **redundant** form **address** signal. A **redundant** form **decoder** decodes **redundant form** data into a **differential** pair of decoded **address** lines for each bit **position** of a **memory address**. **One** of the **two differential** pairs carries correct **address** data. The one **address** line to be used is determined on a memory line by memory line basis, using the address of the memory lines **themselves**. The **redundant** form **address** decoder avoids **a** completion **add** that would otherwise be required, yielding very fast access to memory... ... The present invention provides a memory system (200) that retrieves data based upon **redundant** form **address** data. The memory system (200) includes **a** memory (**220**) having a plurality of memory lines (222) and an address decoder (210) that enables one of the memory lines (222) in response to a **redundant** form **address** signal. A **redundant** form decoder (230) **decodes redundant form** data into **a** differential pair of decoded **address** lines for each bit **position** of a **memory address**. One of the **two differential** pairs carries **correct address** data. The one **address** line to be used is determined on a memory line by memory line basis, using the address of the memory lines themselves. The **redundant** form **address** decoder (230) avoids a completion add **that** would **otherwise** be required, yielding very fast access to memory... ...**Claims:**A memory system (600), comprising:an address decoder (610) adapted to receive **redundant** form **address** signals,a memory (620) populated by memory lines (622), each

memory **line** organized **into** first and second blocks (623, 624), the blocks coupled to the address decoder (610) by... ... A memory system, comprising:an address decoder adapted to receive **redundant** form **address** signals,a memory populated by memory lines, each memory line organized into first and second... Basic Derwent Week: **200029**...

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8/3,K/8 (Item 8 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0009597747 *Drawing available*
WPI Acc no: 1999-546661/**199946**
XRPX Acc No: N1999-405823
Defective relief circuit for semiconductor memory device - generates repair enable signal which drives redundant circuit in memory, when logic address corresponds to address of defective cell
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: CHOI Y J

Patent Family (6 patents, 4 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
JP 11238393	A	19990831	JP 1998289680	A	19981012	199946	B
US 6091649	A	20000718	US 1998173294	A	19981014	200037	E
KR 1999069338	A	19990906	KR 19983510	A	19980206	200046	E
TW 384482	A	20000311	TW 1998113675	A	19980819	200052	E
KR 265765	B1	20001002	KR 19983510	A	19980206	200134	E
JP 3708726	B2	20051019	JP 1998289680	A	19981012	200569	E

Priority Applications (no., kind, date): KR 19983510 A 19980206

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
JP 11238393	A	JA	9	6		
KR 1999069338	A	KO		6		
TW 384482	A	ZH				
JP 3708726	B2	JA	10		Previously issued patent	JP 11238393

Original Publication Data by AuthorityArgentina**Publication No. Original Abstracts:**An integrated circuit memory device includes a memory access circuit operative to generate an **address**. A **redundant** memory is responsive to the memory access circuit and has a plurality of memory locations... **Claims:**An integrated circuit memory device, comprising:a memory access circuit operative to generate an **address**;a redundant memory having a **plurality** of **memory locations**, said redundant **memory** providing **access to** one of **a** first **memory location** or a second **memory location responsive** to an address **applied thereto**, wherein one of the first or second memory locations is accessed based on a redundancy... ... a mode control signal, said self-testing redundancy control circuit operative to apply a received **address** to said **redundant** memory in said normal **mode** and to **apply** an internally generated test **address** to said **redundant** memory in said BIST **mode**, said self-**testing** redundancy control circuit operative to apply said redundancy control signal to said redundant memory based on a received **address** in **said** normal mode.... Basic Derwent Week: **199946**...

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8/3,K/9 (Item 9 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0008906757 *Drawing available*
WPI Acc no: 1998-456505/**199839**
XRPX Acc No: N1998-356258
Memory device e.g. EEPROM with selective redundancy - has switch to connect one of memory cells of second memory array, detachably coupled to corresponding memory cell of first memory array and to disconnect them selectively for accessing address location

Patent Assignee: MICROCHIP TECHNOLOGY INC (MICR-N)
Inventor: YACH R L

Patent Family (2 patents, 20 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5793684	A	19980811	US 1997891348	A	19970710	199839	B
WO 1999003105	A1	19990121	WO 1997US23064	A	19971129	199910	E

Priority Applications (no., kind, date): US 1997891348 A 19970710

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 5793684	A	EN	5	1	
WO 1999003105	A1	EN			
National Designated States,Original	JP KR				
Regional Designated States,Original	AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE				

Alerting Abstract ...cells (14), so that a user is allowed to connect them together, for producing one **redundant** memory cell **address** location for storing data and to disconnect them mutually, to increase the total number of... Original Publication Data by AuthorityArgentina**Publication No.** ...**Original Abstracts:**high reliability. The memory device has two memory arrays wherein both memory arrays have a **plurality of** address **locations** for storing **data**. A switching unit is used to removeably connect the address **locations** of the first **memory array** means to **corresponding address locations** of second **memory array** in order **to produce** a first memory array having **redundant address** locations. If **high reliability** and redundancy is not required, a signal may be sent to the switching unit to... ... amount of address locations for storing data as compared to the first memory array having **redundant address** locations. ... ... high reliability. The memory device has two memory arrays (12, 18) wherein both memory arrays **have a plurality** of **address locations** for **storing data**. A switching **unit** (24) **is** used to removably connect the address **locations** of the first **memory** array (12) to corresponding address locations of second memory array (18) in order to produce a first memory array having **redundant address** locations. If high reliability and redundancy is **not required**, a signal maybe sent to the switching unit (24) to disconnect the address locations of... ... of address locations for storing data as compared to the first memory array (12) having **redundant address** locations. ...**Claims:**combination: first memory array means for storing data wherein said first memory array means comprises **a** plurality of address locations; second memory array **means** for storing data **wherein** said second memory array means comprises a plurality **of address locations** and having at least one of said plurality of address **locations** of said second **memory array means** removeably coupled to **a corresponding** address **location** of said first **memory array means**; Input/Output (I/**O**) decode means coupled to said first memory array means and to said second memory array... ... second memory array means; and switching means coupled to said at least one of said **plurality** of **address locations** of said second **memory** array means **removeably** coupled **to said** corresponding address **location of said** first **memory** array means for allowing a **user** to connect said at least one of said **plurality** of **address locations** of said second **memory** array means **to** said **corresponding address location** of said **first memory** array means for producing at **least** one redundant address **location for** storing said data and for allowing **said user** to disconnect said at least one of said **plurality** of **address locations** of said second **memory** array means **from** said **corresponding address location** of said **first memory** array means to increase a **total** number of address **locations of** said **memory** device for storing said data. ... Basic Derwent Week: **199839**...

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8/3,K/10 (Item 10 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0007639927 *Drawing available*
WPI Acc no: 1996-258872/**199626**
XRPX Acc No: N1996-217872
Retaining and retrieval device for storage and retrieval of ladder - includes primary mounting bracket fixedly secured to vehicle shelf area, primary link arm pivotally secured to first securement post, and longitudinally extensible arm pivotally secured to second securement post
Patent Assignee: ZIAYLEK M P (ZIAY-I); ZIAYLEK T (ZIAY-I)
Inventor: ZIAYLEK M P

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5518357	A	19960521	US 1994274530	A	19940713	199626	B

Priority Applications (no., kind, date): US 1994274530 A 19940713

Patent Details					
Patent Number	**Kind**	**Lan**	**Pgs**	**Draw**	**Filing Notes**
US 5518357	A	EN	10	7	

Original Publication Data by AuthorityArgentina**Publication No.** ...**Original Abstracts:**of the ladder to extend therein for securement. The retaining apparatus is mounted by a **plurality** of brackets and **link** arms to easily **allow** movement between the retrieval and the **storage position**. These arms **also maintain** the upper area of the ladder above the lower portion of the ladder such that... ...**Claims:**vehicle shelf area in a location spatially disposed from said primary mounting bracket; G. a **secondary link arm pivotally** secured with respect to said secondary mounting bracket and extending outwardly therefrom; H. a driveshaft attached to said primary **link** arm **and** said **secondary link arm to** facilitate pivotal movement of said **secondary link arm responsive** to pivotal movement of said primary link arm responsive to extension and retraction of said... ... Basic Derwent Week: **199626**...

Dialog eLink: Order File History
8/3,K/11 (Item 11 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0006148856 *Drawing available*
WPI Acc no: 1992-391632/**199248**
XRPX Acc No: N1992-298722
Extending physical system addressable memory - using secondary storage subsystem controller which intercepts requests to non-existent RAM and translates them into requests for data from cheaper secondary memory
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: BEALKOWSKI R

Patent Family (3 patents, 5 countries)							
Patent Number	**Kind**	**Date**	**Application Number**	**Kind**	**Date**	**Update**	**Type**
EP 515046	A1	19921125	EP 1992303836	A	19920428	199248	B
CA 2066542	A	19921125	CA 2066542	A	19920421	199307	E
US 5873129	A	19990216	US 1991705277	A	19910524	199914	E
			US 1994203729	A	19940228		

Priority Applications (no., kind, date): US 1991705277 A 19910524; US 1994203729 A 19940228

Patent Details						
Patent Number	**Kind**	**Lan**	**Pgs**	**Draw**	**Filing Notes**	
EP 515046	A1	EN	11	4		
Regional Designated States,Original	DE FR GB					
CA 2066542	A	EN				
US 5873129	A	EN			Continuation of application	US 1991705277

Original Publication Data by AuthorityArgentina**Publication No.** ...**Claims:**A computer having a processor (202), a physical RAM (264) having a fixed address range, **a** bus (230) and **secondary** storage (106) accessible by way of the bus, characterised in that the computer further comprises... ... for coupling the central processor to the physical RAM;secondary storage coupled to the bus;**address** decoder means for **determining** whether a read/write request for RAM is beyond the fixed address range of the physical RAM; anda **secondary** storage controller circuit, **coupled** to the bus, comprising:a secondary storage manager to read/write emulated RAM on the... ... RAM on the secondary storage and control reading and writing of emulated RAM by the **secondary storage** manager; whereby RAM storage **addresses** beyond the fixed **address range** of physical RAM addresses can be used by the processor, thereby extending the address range... ... Basic Derwent Week: **199248**...

Dialog eLink: Order File History
8/3,K/12 (Item 12 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0003402899
WPI Acc no: 1985-171427/**198528**
Semiconductor dynamic RAM for video display graphics - separates random memory access operations from sequential memory access operations in serial scanning
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: THREEWITT B N; THREEWITT N; THREEWITT N B

Patent Family (6 patents, 11 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 1985002935	A	19850704	WO 1984US1718	A	19841022	198528	B
EP 166739	A	19860108	EP 1984904234	A	19841022	198602	E
JP 61500813	W	19860424	JP 1984504100	A	19841022	198623	E
US 4608678	A	19860826	US 1983564969	A	19831223	198637	E
EP 166739	B1	19920520	EP 1984904234	A	19841022	199221	E
			WO 1984US1718	A	19841022		
DE 3485742	G	19920625	DE 3485742	A	19841022	199227	E
			EP 1984904234	A	19841022		
			WO 1984US1718	A	19841022		

Priority Applications (no., kind, date): US 1983564969 A 19831223

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
WO 1985002935	A	EN	18	3		
National Designated States,Original	JP					
Regional Designated States,Original	AT BE CH DE FR GB LU NL SE					
EP 166739	A	EN				
Regional Designated States,Original	AT BE CH DE FR GB LI LU NL SE					
EP 166739	B1	EN	13		PCT Application	WO 1984US1718
					Based on OPI patent	WO 1985002935
Regional Designated States,Original	AT BE CH DE FR GB LI LU NL SE					
DE 3485742	G	DE			Application	EP 1984904234
					PCT Application	WO 1984US1718
					Based on OPI patent	EP 166739
					Based on OPI patent	WO 1985002935

Equivalent Alerting Abstract ...The addressor is disposed for providing the secondary memory with a start **address** within the **secondary** memory. The start **address** indicates a predetermined bit position within the secondary memory at which predetermined bit position a... **Technology Focus** Original Publication Data by AuthorityArgentina**Publication No.** ...**Original Abstracts:**invention is implemented by utilizing a secondary memory means in conjunction with parallel loadable, multiple-**bit address** counters... ... implemented by utilizing a secondary memory means (26) in conjunction with parallel loadable, multiple-bit **address** counters (38 **and** 40). ...**Claims:**device, the semiconductor memory device comprising:
a main memory (24) having a plurality (n) of **address** input terminals;
a **secondary** memory (26) including two shift registers in the form of two random access memory means... ... access to either shift register under the control of a select signals, beginning at an **arbitrary** bit **position**, said presettable address counter means (38,**40**) having a **plurality** of input terminals and a plurality of output terminals (49,51) coupled to said shift... ... Basic Derwent Week: **198528**...

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8/3,K/13 (Item 13 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0003272171
WPI Acc no: 1985-031953/**198505**
Memory management system for computer - simultaneously fetches virtual address and access protection code from secondary memory and stores them in two addressable memories
Patent Assignee: NCR CORP (NATC)
Inventor: CELIO J A

Patent Family (7 patents, 5 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 1985000232	A	19850117	WO 1984US950	A	19840622	198505	B
EP 146623	A	19850703	EP 1984902651	A	19840622	198527	E
JP 60501628	W	19850926	JP 1984502510	A	19840622	198545	E
US 4580217	A	19860401	US 1983506923	A	19830622	198616	E
CA 1209715	A	19860812				198637	E
EP 146623	B	19871111	EP 1984902651	A	19840622	198745	E
DE 3467436	G	19871217				198751	E

Priority Applications (no., kind, date): US 1983506923 A 19830622

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
WO 1985000232	A	EN	36	5	
National Designated States,Original	JP				
Regional Designated States,Original	DE FR GB				
EP 146623	A	EN			
Regional Designated States,Original	DE FR GB				
CA 1209715	A	EN			
EP 146623	B	EN			
Regional Designated States,Original	DE FR GB				

Equivalent Alerting Abstract ...comprises a protection code storage device for storing protection codes. The store has several code **storage locations** with each of the locations corresponding to one of **several address storage locations**. A protection code interrogator interrogates each of the **storage locations** for a predetermined code. The code interrogator operation is simultaneous with the operation of an... **Technology Focus** Original Publication Data by AuthorityArgentina**Publication No. Original Abstracts:**A virtual address and access protection code stored at that address are fetched simultaneously **from secondary** memory and stored in corresponding locations in first and second content addressable memories (36, 68... ... A virtual address and access protection code stored at that address **are** fetched simultaneously from **secondary** memory and stored **in** corresponding locations in first and second content addressable memories. When a program-generated virtual address... ... A virtual address and access protection code stored at that address are fetched simultaneously from **secondary memory** and stored in corresponding locations in first and second content addressable memories (36, 68). When... ... Basic Derwent Week: **198505**...

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8/3,K/14 (Item 14 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0001415096
WPI Acc no: 1977-H5351Y/**197736**
Memory module with selectable byte addressing - has multiple location data and address memories for digital data processing system

Patent Assignee: NIPPON DIGITAL EQUIP KK (DIGI)
Inventor: GIGGI R; LEVY J V; NORTHRUP T A

Patent Family (1 patents, 1 countries)							
Patent Number	**Kind**	**Date**	**Application Number**	**Kind**	**Date**	**Update**	**Type**
US 4045781	A	19770830	US 1976658071	A	19760213	197736	B

Priority Applications (no., kind, date): US 1976658071 A 19760213

...**has multiple location data and address memories for digital data processing system Alerting Abstract** ...The associative memory unit contains a **multiple location address memory** and a **multiple location address memory** and a **multiple location** data **memory**. There is a correspondence between each address location and a data location. Each time a... Original Publication Data by AuthorityArgentina**Publication No.** ...**Original Abstracts:**memory unit and a random access back-up unit. The associative memory unit contains a **multiple location address memory** and a **multiple location** data **memory** wherein there is a correspondence between each address location and a data location. Each time... ... data to locations in the back-up memory unit, and such a device transmits an **address** to the **back-up** memory unit during such transfers. If the associative memory unit contains data from a corresponding... ... Basic Derwent Week: **197736**...